AMENDMENTS TO THE CLAIMS

This listing of claims replaces all prior versions of claims in the application.

1-12. (Cancelled)

13. (Currently amended): A method of fabricating a circuit substrate, said circuit substrate having any of a passive element and an interconnection pattern, said passive element comprising at least one of a dielectric film, a resistance film and a conductor film, said method comprising a film forming step,

said film forming step forming at least one of said dielectric film, said resistance film and said conductor film by generating and ejecting dry aerosol consisting essentially of a fine solid particle material together with a carrier gas, said dry aerosol being ejected into a reduced pressure environment of a pressure lower than a pressure in an aerosol generator generating said dry aerosol, with a speed of 200-400m/second such that said fine solid particle material causes impact activation upon impact upon said circuit substrate,

said film forming step for forming at least one of said dielectric film, said resistance film and said conductor film being conducted by generating and ejecting dry aerosol of a fine and brittle solid particle material together with said carrier gas.

14. (Original): The method as claimed in claim 13, wherein said circuit substrate includes a base substrate and an insulation layer laminated on said base substrate,

at least one of said base substrate and said insulation layer comprises a resin material.

15. Cancelled.

16. (Original): The method as claimed in claim 13, wherein said carrier gas comprises at least one of a helium gas, a neon gas, an argon gas and a nitrogen gas.

17. (Original): The method as claimed in claim 13, wherein said fine particle material comprises fine particles having an average diameter of 10nm – 1μm.

18. (Original): The method as claimed in claim 13, wherein said resin material comprises at least one of an epoxy resin, a polyimide resin, a polyester resin, a fluorocarbon copolymer, and a fiber glass.

19. (Original): The method as claimed in claim 13, further comprising a planarizing step for planarizing a surface of any of said dielectric film, resistance film and conductor film after said film forming step.

20-46. (Cancelled)

47. (Currently amended): A fabrication method of a circuit substrate in which an interlayer insulation film and a conductor layer are laminated, comprising the steps of:

forming said interlayer insulation film by generating and spraying dry aerosol consisting essentially of a fine and brittle solid particle material together with a carrier gas, said dry aerosol being ejected into a reduced pressure environment of a pressure lower than a pressure in an aerosol generator generating said dry aerosol, with a speed of 200-400m/second such that said fine solid particle material causes impact activation upon impact upon said circuit substrate; and

forming said conductor layer while depositing a metal or an alloy thereon.

48. (Previously presented): The method as claimed in claim 47, wherein said step of forming said conductor layer is conducted by using any of a non-electrolytic plating process, an electrolytic plating process, a sputtering process, a vacuum evaporation deposition process and a CVD process.

49. (Previously presented): The method as claimed in claim 47, further comprising the step of forming a connection hole in said interlayer insulation film by using a hydrofluoric acid while masking said interlayer insulation film.

50. (Previously presented): A method of fabricating a circuit substrate, said circuit substrate having any of a passive element and an interconnection pattern, said passive element comprising at least one of a dielectric film, a resistance film and a conductor film, said method comprising a film forming step,

said film forming step forming at least one of said dielectric film, said resistance film and said conductor film by impact activation of a fine solid particle material sprayed with a carrier gas in the form of aerosol into a reduced pressure environment of a pressure lower than a pressure in an aerosol generator generating said dry aerosol, said dry aerosol being ejected into said reduced pressure environment with a speed of 200-400m/second.

51. (Previously presented): A fabrication method of a circuit substrate in which an interlayer insulation film and a conductor layer are laminated, comprising the steps of:

forming said interlayer insulation film by impact activation of a fine solid particle material sprayed with a carrier gas in the form of aerosol into a reduced pressure environment of

a pressure lower than a pressure in an aerosol generator generating said dry aerosol, said dry aerosol being ejected into said reduced pressure environment with a speed of 200-400m/second; and

forming said conductor layer while depositing a metal or an alloy thereon.

52. (New): A method of fabricating a circuit substrate, said circuit substrate having any of a passive element and an interconnection pattern, said passive element comprising at least one of a dielectric film, a resistance film and a conductor film, said method comprising a film forming step, said film forming step forming at least one of said dielectric film, said resistance film and said conductor film by forming a resist pattern on said circuit substrate and spraying dry aerosol while using said resist pattern as a mask, wherein said spraying dry aerosol comprises generating and ejecting dry aerosol consisting essentially of a fine solid particle material together with a carrier gas, said dry aerosol being ejected into a reduced pressure environment of a pressure lower than a pressure in an aerosol generator generating said dry aerosol, with a speed of 200-400m/second such that said fine solid particle material causes impact activation upon impact upon said circuit substrate.

53. (New): A fabrication method of a circuit substrate in which an interlayer insulation film and a conductor layer are laminated, comprising the steps of:

forming a resist pattern on said circuit substrate and forming said interlayer insulation film by spraying dry aerosol while using said resist pattern as a mask,

wherein said spraying dry aerosol comprises generating and spraying dry aerosol consisting essentially of a fine solid particle material together with a carrier gas, said dry aerosol being ejected into a reduced pressure environment of a pressure lower than a pressure in an aerosol generator generating said dry aerosol, with a speed of 200-400m/second such that said fine solid particle material causes impact activation upon impact upon said circuit substrate; and

forming said conductor layer while depositing a metal or an alloy thereon.

54. (New): A method for fabricating a circuit substrate having at least a capacitor, said method comprising the steps of:

forming, on a resin insulation film, a lower electrode pattern;

forming a dielectric film on said lower electrode pattern; and

forming an upper electrode pattern on said dielectric film,

said step of forming said dielectric film comprising generating and ejecting dry aerosol of fine ceramic particles together with a carrier gas, said dry aerosol being ejected into a reduced pressure environment of a pressure lower than a pressure in an aerosol generator generating said dry aerosol, with a speed of 200-400m/second such that said fine ceramic particles cause impact activation upon impact to said lower electrode.

55 (New) The method as claimed in claim 54, further comprising the step of forming a resist pattern on said lower electrode pattern so as to expose a part of said lower electrode pattern, and wherein said step ejecting said dry aerosol is conducted while using said resist pattern as a mask.